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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,529	04/12/2004	Jens Braun	INFN 2294-US	3329

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EXAMINER	
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ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 11/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/822,529	BRAUN, JENS	
	Examiner	Art Unit	
	Saqib J. Siddiqui	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *5,16 and 19-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-15,17 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's response was received and entered September 05, 2006.

- Claims 1-21 are pending.
- Claims 1, 8-9, 12 & 18 are amended.
- Claims 5, 16, 19-21 are canceled
- Application is currently pending.

Response to Amendment

Applicant's arguments and amendments with respect to claims 1-21 filed September 05, 2006 have been fully considered but they are not persuasive. The Examiner would like to point out that this action is made final (See MPEP 706.07a).

Applicant contends that the prior arts of record do not teach providing signals, utilizing a self-test control device located within the DRAM memory chip to a control input of the DRAM memory chip and a control input at the nonvolatile memory chip; and disconnecting control input signals from outside the multichip memory module using the self-test control device. Examiner respectfully disagrees.

As per US Pat no. 6,971,051 B2 Taylor et al. teaches "The self-tester capability includes stored test code that is specific to detecting errors within the information (e.g., executable code) residing within the volatile memory. The stored test code includes instructions, which implement memory-testing routines. The test code may be stored within embedded non-volatile memory of the integrated circuit.... Error correction is a

possibility in the case that a code error condition is detected, but the preferred method is one in which the device reinitializes itself from the non-volatile memory and the information (e.g., executable code) is reloaded to the volatile memory." (column 3, lines 1-35). Here clearly Taylor et al. teaches that the self-test capabilities are located within the volatile memory. Upon testing and error correction code reinitializes by sending signals to the non-volatile and volatile memory. Further Taylor et al. merely states that in an alternative embodiment the isolation can be performed by CRC, which is off-chip. However, that is just an alternative embodiment and the function of isolation can be performed by the self-test controller as it also includes the instructions to perform CRC. "In one embodiment, the volatile memory check consists of calculating a cyclic redundancy check (CRC) or checksum of the entire code space of the DRAM." (columns 5-6, lines 55-10). Also, Taylor clearly states that "the memory management techniques can be extended to stand-alone volatile memory chips," (column 7, lines 10-20), hence not disconnecting from outside the stand-alone volatile memory chip.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 12-15 & 17 are rejected under 35 U.S.C. 112, second paragraph.

Amended claim 12 recites the limitation "second switching device" in claim 12. There is insufficient antecedent basis for this limitation in the claim.

As per claims 13-15 & 17:

These claims are rejected by virtue of their dependency.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-2, 6, and 11 are rejected under 35 U.S.C. 102(e) as being fully anticipated by Taylor et al. (Taylor hereinafter) US Pat no. 6,971,051 B2.

As per claim 1:

Taylor teaches a method for testing memory cells of a DRAM memory chip arranged together with a non-volatile memory chip in a multichip memory module incorporated in an application apparatus, comprising (Figure 4, column 1, lines 15-65): conducting a self-test of the memory cells of the DRAM memory chip in a time period during which the memory cells of the DRAM memory chip are not accessed in an operative operating mode of the application apparatus (column 2, lines 40-67); providing signals (Figure 4), utilizing a self-test control device (column 6, lines 35-40), to a control input of the DRAM memory chip and a control input at the nonvolatile memory chip

(column 6, lines 35-65); and disconnecting control input signals from outside the multichip memory module (Figure 3 # 36, column 6, lines 25-35).

As per claim 2:

Taylor teaches the method as rejected in claim 1 above, further comprising: initiating the self-test by a central processing unit of the application apparatus, the central processing unit arranged outside the multichip memory module (Figure 4 # 40).

As per claim 6:

Taylor teaches the method as rejected in claim 1 above, further comprising selecting addresses of the DRAM memory chip to test memory cells utilizing a self-test control device disposed in the DRAM memory chip (column 6, lines 5-45).

As per claim 11:

Taylor teaches the method as rejected in claim 1 above, wherein the self-test is conducted in a period from at least one of: during a battery charging period of the application apparatus; during a standby period of the application apparatus; after a battery change of the application apparatus; after an initial switch-on of the application apparatus; after a switch-off of the application apparatus; and according to a time schedule stored in the nonvolatile memory chip (column 5, lines 3-21).

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 3-4, 7-8, and 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor US Pat no. 6,971,051 B2, and further in view of Barr US Pat no. 5,758,056.

As per claim 3:

Taylor substantially teaches a method for testing memory cells of a DRAM memory chip arranged together with a non-volatile memory chip in a multichip memory module incorporated in an application apparatus, comprising (Figure 1): conducting a self-test of the memory cells of the DRAM memory chip in a time period during which the memory cells of the DRAM memory chip are not accessed in an operative operating mode of the application apparatus (column 2, lines 30-67), wherein a data bus of the DRAM memory chip and a data bus of the nonvolatile memory chip are connected (Figure 4 # 64).

Taylor does not explicitly teach storing addresses of defective memory cells in the nonvolatile memory chip.

However, Barr in an analogous art teaches storing addresses of defective memory cells in the nonvolatile memory chip (Figure 1 # 16, column 4, lines 1-31). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to enable the Taylor's invention to store the exact location of the defective memory cell, as it would have enabled the recovery module in Taylor's invention to correct the exact error cell as opposed to resetting the whole DRAM, which

would significantly cut down the testing time. Further it should be noted that recovering defective addresses and storing them is commonly known in the art and is used repeatedly specially when memory testing is involved.

As per claim 4:

Taylor/Barr teach the method as rejected in claim 3 above except for explicitly stating the switching means to deactivate or activate the bus. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a method to deactivate the data bus, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* USPQ 233.

As per claim 7:

Taylor/Barr substantially teaches the method as rejected in claim 3 above.

Taylor does not explicitly teach selecting addresses of the non-volatile chip to store the defective addresses of the DRAM.

However, Barr in an analogous art teaches selecting addresses of the nonvolatile memory chip to store the addresses of the defective memory cells of the DRAM memory chip utilizing a central processing unit (Figure 1 # 11, column 4, lines 1-65). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to enable the Taylor's invention to store the exact location of the defective memory cell, as it would have enabled the recovery module in Taylor's invention to correct the exact error cell as opposed to resetting the whole DRAM, which would significantly cut down the testing time. Further it should be noted that recovering

defective addresses and storing them is commonly known in the art and is used repeatedly specially when memory testing is involved.

As per claim 8:

Taylor/Barr substantially teaches the method as rejected in claim 7 above wherein the addresses of the defective memory cells are read from the nonvolatile memory chip by the central processing unit in the operative operating mode of the application apparatus (Taylor, column 5, lines 40-57 & Barr column 3, lines 25-65).

As per claim 9:

Taylor/Barr substantially teaches the method as rejected in claim 8 above except for explicitly stating skipping the defective memory addresses. It would have been obvious to one of ordinary skill in the art at the time the invention was made to skip the defective addresses, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* USPQ 233.

As per claim 10:

Taylor substantially teaches a method for testing memory cells of a DRAM memory chip arranged together with a non-volatile memory chip in a multichip memory module incorporated in an application apparatus, comprising (Figure 1): conducting a self-test of the memory cells of the DRAM memory chip in a time period during which the memory cells of the DRAM memory chip are not accessed in an operative operating mode of the application apparatus (column 2, lines 30-67).

Taylor does not explicitly teach the replacement of defective memory cells with redundant memory cells in the DRAM memory chip.

However, Barr in an analogous art teaches the replacement of defective memory cells with redundant memory cells in the DRAM memory chip (Figure 1 # 18, column 3, lines 25-60). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to enable the Taylor's invention to replace the defective addresses with redundant memory cells, as it would have enabled Taylor's invention to correct the exact error cell as opposed to resetting the whole DRAM, which would significantly cut down the testing time. Further it should be noted that replacing defective addresses using redundant cells sis commonly known in the art and is used repeatedly in the art specially when memory testing is involved.

As per claims 12-15 & 17:

Claims 12-15 & 17 are directed to an apparatus of the method of Claims 1-11. Taylor, Lai and Barr teach, either alone or in combination as stated above, the method as set forth in Claims 1-11. Therefore, Taylor, Lai and Bar also teach, either alone or in combination as stated above, an apparatus as set forth in Claims 12-17.

As per claim 18:

Claim 18 is directed to means of the method of Claims 1-11 and apparatus of claims 12-17. Taylor, Lai and Barr teach, either alone or in combination as stated above, the method as set forth in Claims 1-11 and apparatus as set forth in Claims 12-17. Therefore, Taylor, Lai and Bar also teach, either alone or in combination as stated above, the means as set forth in Claim 18.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Examiner's Note: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are

applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

Saqib Siddiqui
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11/03/2006

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